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LOW POWER ARITHMETIC CIRCUITS USING FINFET DEVICE IN 32NM TECHNOLOGY

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ABSTRACT

Aim: *A low power computing device design is the objective of the work. The objective is met using FinFET and inexact computing methods. A FinFET based arthmetic circuits for the processing element units in DSP application is to be designed and proposed.* ***Materials and methods:*** *The circuits are modelled using predictive technology models in 32nm FinFET technology. The proposed arthmetic circuits are a half adder, a full adder and a multiplier. A 4-2 compressor based multiplier is proposed in this paper which reduces the number of operands and partial products. Using compressors for the multiplier reduces the number of interconnects and components.* ***Results:****The proposed FinFET based circuits reduces the leakage current which ultimately results in the reduction of power consumption. As CMOS circuits performance reduces when fabricated below 45nm technology , FinFET devices is the alteranative solution. This work embasis on the design of circuits using FinFET.* ***Conclusion:*** *The proposed circuits are compared with the existing counterparts and found that the performance improvement is 96% on average with the existing CMOS circuits . The modelling and simulations were carried out using Synopsis HSPICE.*

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KEY WORDS

FinFET, Adder, Multiplier, Compressor, Processing Element

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INTRODUCTION

The CMOS based circuits for signal and image processing algorithm was dominating the integrated circuit world upto 90nm technology. The CMOS performance degrades due to leakage current and lower output swing below 90nm. The reduction of supply voltage is not effective. This reduces the driving capability when implemented for arithmetic and logic blocks used in Digital Signal Processing (DSP). The other issues involved are the Short Channel Effects, (SCE), Sub–Threshold Leakage (STL) device variations and gate dielectric leakage [1]. So the gate terminal control is to be taken care which is possible only by having multigate device. The multigate devices also work in different modes [2] and mock the operation of CMOS in short gated mode but with good operability conditions. When arithmetic circuits were designed by these devices the performance is better. Several works are carried out in the implementation of arithmetic circuit using FinFET. The result shows that the leakage and delay analysis are improved when compared to CMOS in an array multiplier is implemented. A low leakage MUX/XOR logics are implemented using symmetric and asymmetric FinFET in literature [3]. A 65% improvement in leakage and 45% in delay is reported.

INEXACT COMPUTING/COMPRESSION

In digital processing where inexact computing becoming an attractive paradigm and VLSI implementation becomes much easier. Then complex arithmetic operations like Fourier analysis or discrete wavelet transform are to be performed the inexact computing becomes more efficient. The inexact computing circuit becomes viable for real time circuits through compressors. The truth table of the compressors is given in Table 1. It can be observed

that the carry output is equal to c_{in} in 24 out of 32 states while the carry is simplified for other 8 outputs.the value.The gate level compressor design for the truth table in table 1 is given in Figure 1(a). The respective multiplier is given in Figure 1(b).

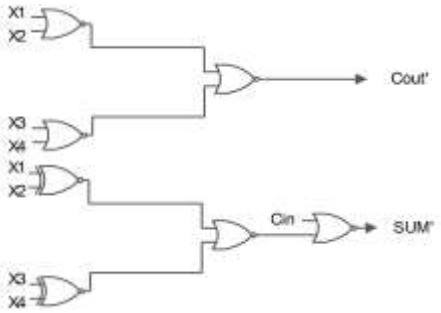

Figure. 1(a): Gate level Implementation of Compressor type 1

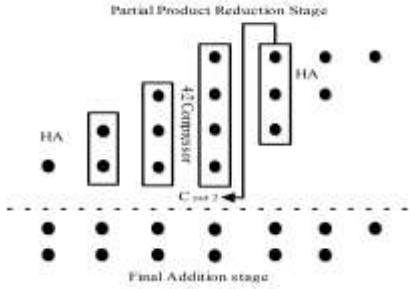

Figure. 1(b): Existing Compressor based Multiplier type 1

An another type of approximate compressor is shown in Figure 2(a) and its multiplier in Figure 2(b). The second compressor reduces the approximate error when compared to the first one. The truth table is given in Table 2.

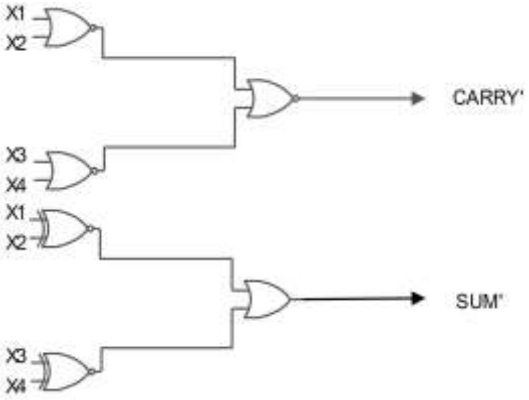

Figure. 2(a): Gate level Implementation of Compressor type 2

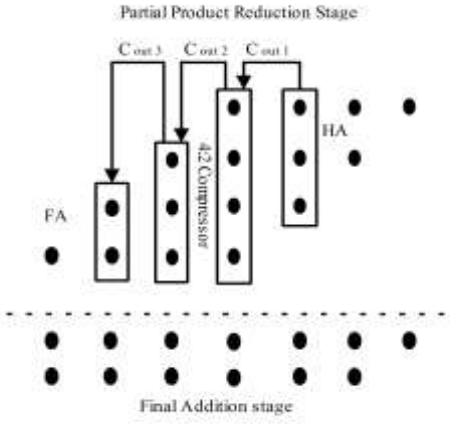

Figure. 2(b): Existing compressor based Multiplier type 2

TABLE I. TRUTH TABLE OF 4-2 COMPRESSOR TYPE 1

Cin	X4	X3	X2	X1	Cout	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

Compressor circuits were initially used for generating partial products in BiCMOS technology [4] and BiCMOS circuit provided better power consumption but failed in the reduction of leakage current. Pass transistors were used for the design. A pass transistor based CMOS multiplier using compressor was reported in the literature [5] and [6]. The compressors have different configuration and best suited for the systems where the noise components are more.

TABLE II. TRUTH TABLE OF 4-2 COMPRESSOR TYPE 2

Cin	X4	X3	X2	X1	Cout'	Carry'	Sum'
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	1
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	0	1
1	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	0	1	1	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	0	1	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	0

Even though the approximate computing reduces accuracy in hard real time systems where speed is pre-dominant factor accuracy can be compromised a little bit. The power and delay reduction can be achieved with significant accuracy [7]. Chip-Hong Chang et al [8] proposed a carry generator circuit to implement a 4-2 and 5-2 compressor cell to operate in tree structured parallel multiplier which operates at very low supply voltage i.e below 1V. Momeni et al [9] have proposed an approximate compressor for multiplication. The proposed design is implemented in an image processing application using Dadda multiplier. The paper reports that the two new approximate 4-2 compressors significantly reduces the power dissipation, delay and transistor count compared to an exact design. In multiplication intensive computing the compressors seem to be leading replacement for existing exact multiplication methods when multi operands are involved [10]. Realization of the compressors is normally based on XOR/XNOR gates. The decomposition of the XOR/XNOR leads to an optimized design presented in the literature [10]. Improvement in terms of delay about 17%, power by 13% and power-delay-product by 30% is reported. Apart from the modified versions in the existing compressors, high performance 5:2 compressor is designed and arithmetic circuits [11] in the literature [12] have been proposed. The design limits the

carry propagation to a single stage. Apart from the above research hybrid methods of combining magnetic tunnel junction (MTJ) and complementary metal–oxide–semiconductor (CMOS) are done in [13] for a compressor design. Joseph Whitehouse and Eugene John [14] proposed a FinFET based array multiplier with different technologies like 20nm, 16nm, 14nm, 10nm and 7nm. The reported performance is for the implementation of an array multiplier using standard cell 28 transistor full adders.

REDUCTION OF LEAKAGE CURRENT AND LEAKAGE POWER USING FINFET TECHNOLOGY

In conventional CMOS devices below 45nm there are problems in driving capability due to leakage currents and other second channel effects like VT roll off and drain induced barrier lowering. At the onset of FinFET technology many works started moving towards FinFET technology from CMOS. Especially in the short channel territories like 65nm and 45nm FinFET promises to deliver superior levels of scalability needed to design integrated circuits for systems.

Device Structure of FinFET

The device structure of FinFET [15] is shown in Figure 3 (a) and (b). The name signifies a fin like structure in the FET device formed on thin Silicon On Insulator (SOI) finger termed fin. The fin is protected by a silicon fin nitride deposit on a thin pad oxide during gate poly-SiGe etching. The fin acts as a channel and terminates both sides of source and drain. The single gate stacking arrangements on top of vertical gates allows three times surface area for the electrons to travel. Gate work-function tailoring is essential to adjust the threshold voltage. Therefore, for the gate material poly-SiGe has been chosen. The crucial geometric device dimensions are shown in Figure 3. A single poly silicon layer is deposited over a fin. Here fin itself acts as a channel and it terminates on both sides of the source and drain. FinFET consists of two gates: front gate and back gate, source and drain. Front gate is used to control the channel conduction and back gate is used to control the threshold voltage. The labels in the figure stands for Lg: printed gate length, Leff : effective gate length which is determined by the distance of the junctions, Tfin: Height of the fin, Wfin : Width of the fin which is the distance between the gate oxides of the two gates.

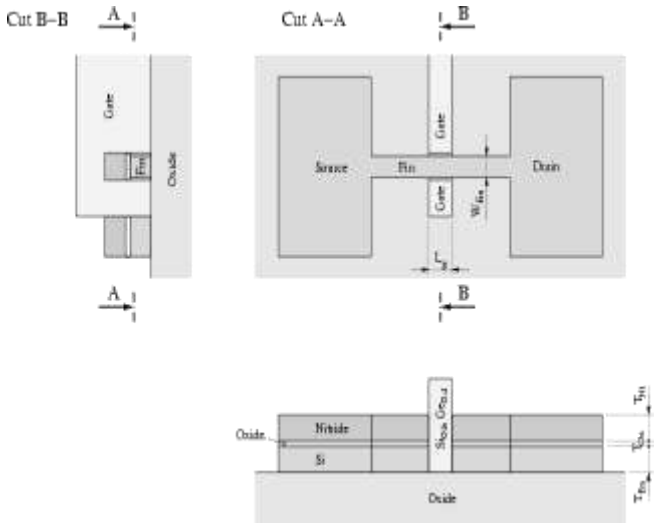

Figure. 3(a): Views of the FinFET Layout

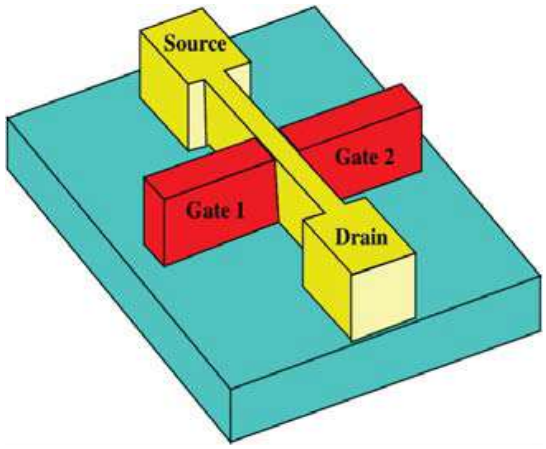

Figure. 3(b): FinFET Device Structure

The tradeoff of designing FinFET's as discrete components due to the issues involved in the manufacturing of similar GATE is rectified by integrated circuit design. From integrated circuits the FinFET technology is moved to the world of System on Chip (SoC) architecture where the complete system is embedded in integrated circuits. As SoCs require very much higher levels of integration and good driving capability FinFET in 35nm technology will be suitable.

PROPOSED COMPRESSOR BASED MULTIPLIER USING FINFET

The implementation of arithmetic circuit using FinFET is effective when analyzing the works available in the literature [16-18]. The conventional method have disadvantage due to the carry propagation and low speed of operation. On the other hand the CMOS based compressor circuit lags in driving capability due to leakage current. These problems are addressed in this paper by proposing a novel FinFET based compressor for multiplier. The design is well suited for any real time DSP application where the driving current should be high. Proposed design can even work under the supply voltage of 1V with good driving capacity. The circuit is faster and delay is reduced. The proposed architecture of Compressor based multiplier using FinFET is given in Figure 4.

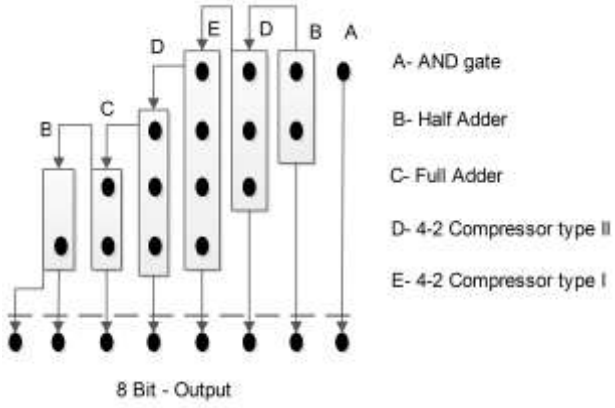

Figure. 4: Architecture of Compressor based Multiplier using FinFET

For the implementation of the multiplier architecture in Figure 4, 2 half adder, 1 full adder and 3 compressors are required.

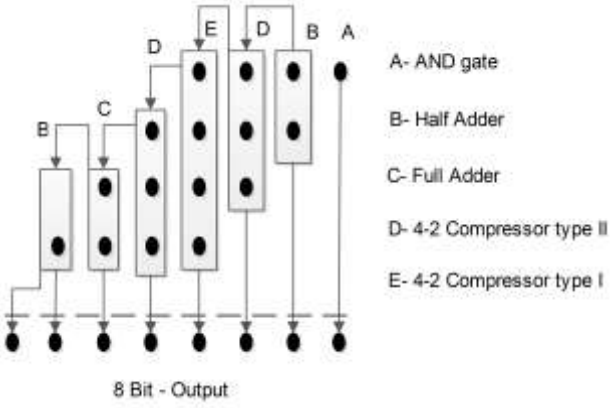

Figure. 5(a): Architecture of Compressor based Multiplier using FinFET

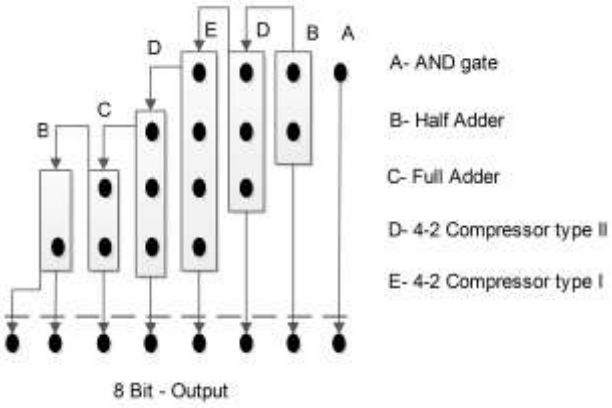

Figure. 5(b): Architecture of Compressor based Multiplier using FinFET

The proposed adder structure is designed using transmission gate which selectively block or pass the data from the input to the output. The proposed 6T half adder and 10T full adder is given in Figure 5.(a) and Figure 5.(b) respectively. The less number of transistors reduces the area and consume lesser power. When considering driving capability the proposed design in FinFET for the lesser transistors have better performance compared to the CMOS counterpart. The CMOS pass transistor logic have lesser output voltage swing due to the threshold voltage defeat problem is rectified in this design. The FinFET based adder not only reduces the power consumption, but may also lead to better switching in the case of cascaded operation such as ripple carry adder. A low V_{DD} operation is also possible, which can work at 0.7V.

IMPLEMENTATION

A FinFET based AND gate implementation and shown in Figure 6(a) and 5(b). For the implementation predictive technology model for 32nm is used.

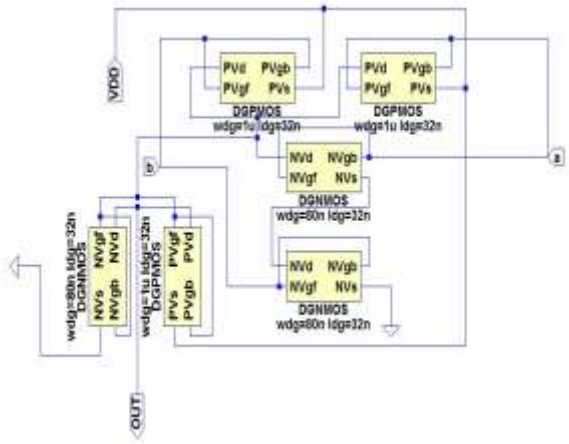

Figure. 6(a): FinFET AND Gate

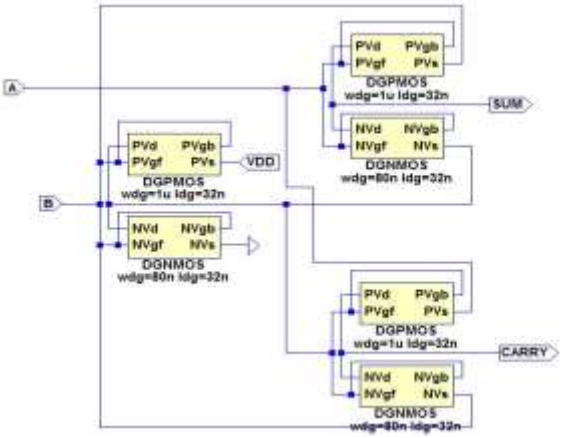

Figure. 6(b): FinFET Proposed Half Adder

The implementation of the proposed full adder is given in Figure 7.The supply voltage applied to the circuit is1V and the proposed full adder implementation was carried out using FinFET Predictive Technology Model (PTM) in 32nm.

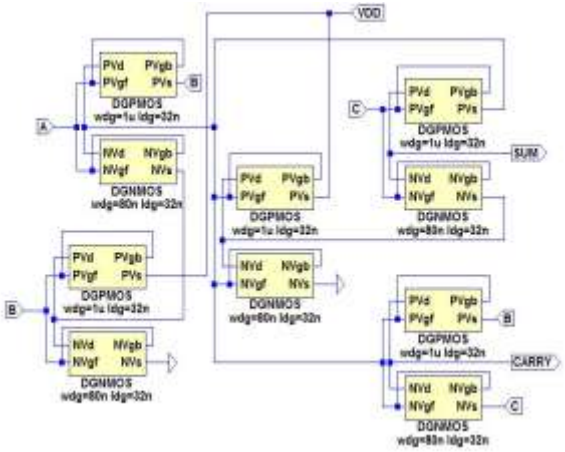

Figure. 7: FinFET Proposed Full Adder

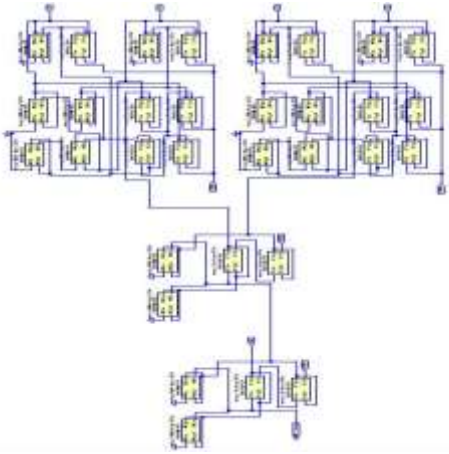

Figure. 8(a): FinFET Compressor type 1 (Sum block)

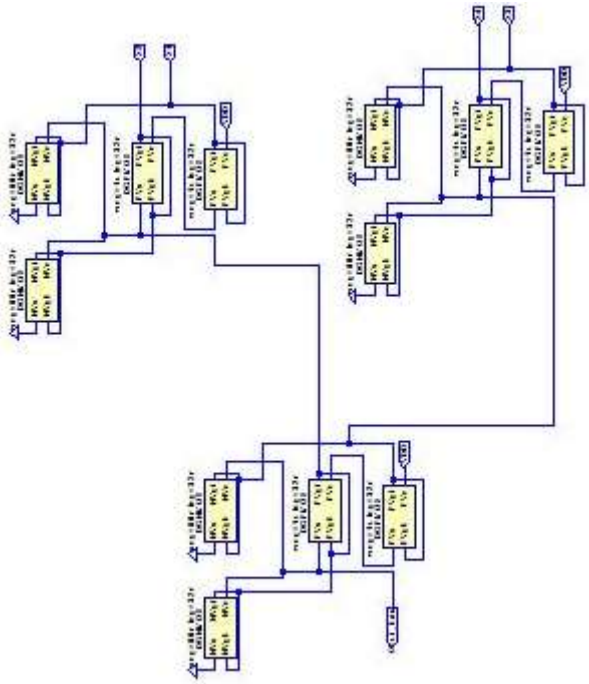

Figure. 8(b): FinFET Compressor type 1 (Carry block)

Figure 8(a) and 8(b) shows the FinFET based Compressor type 1 sum and carry block. Similarly compressor type 2 circuits are given in Figure 9. 4-bit implementation is carried out to validate the performance with respect to both compressor types.

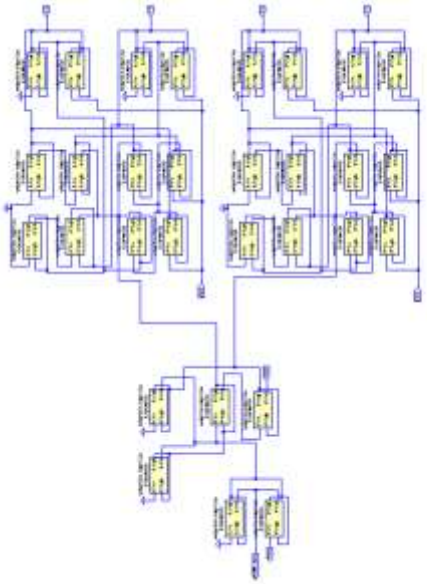

Figure. 9(a): FinFET Compressor type 2 (Sum block)

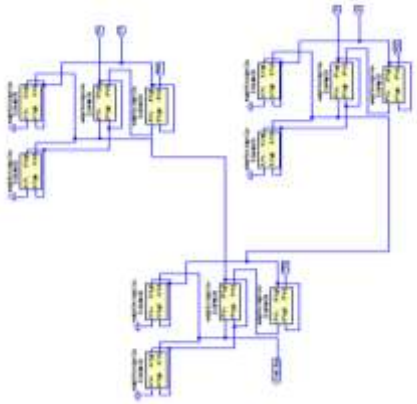

Figure. 9(b): FinFET Compressor type 2 (Carry block)

The conventional array multiplier implemented is shown in Figure 10. The compressor type 1 and type 2 based systolic array multiplier are given in Figure 11 and Figure 12 respectively.

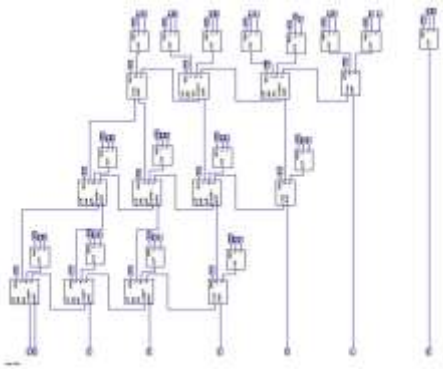

Figure. 10: Conventional Array Multiplier for Systolic Architecture

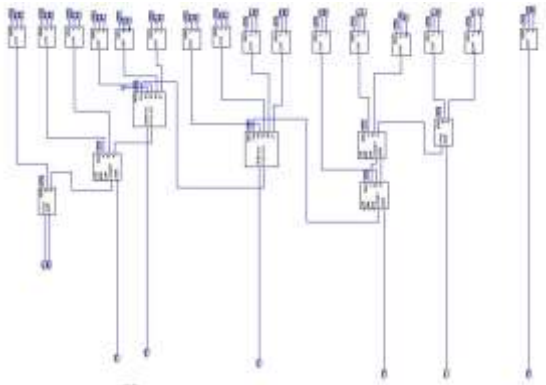

Figure. 11: Compressor Type 1 based Array Multiplier for Systolic Architecture

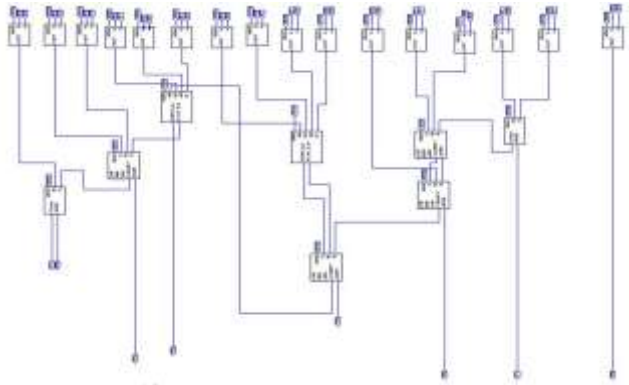

Figure. 12: Compressor Type 2 based Array Multiplier for Systolic Architecture

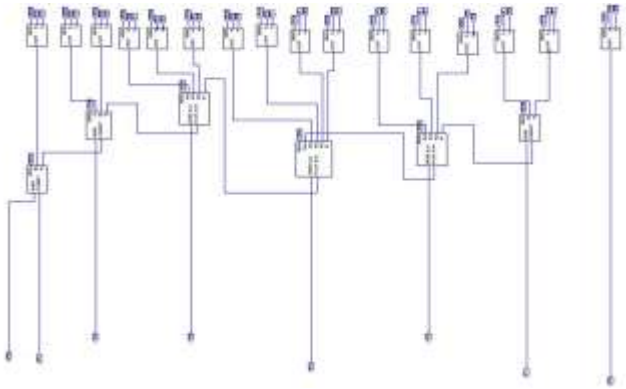

Figure. 13: Proposed Compressor Type 1 and Type 2 based Array Multiplier for Systolic Architecture

The proposed Compressor based Array multiplier for Systolic architecture is shown in figure 13. The proposed multiplier is a hybrid type, In which compressor type 1 and type 2 are used for implementation with the proposed 6T half adder and 10T full adder.

RESULT AND DISCUSSION

The power consumption of different components implemented using CMOS and FinFET is shown in the Table 3. The average power is measured and tabulated. From the results it is observed that the power dissipation in FinFET is 95.46% compared to CMOS. Especially in comparison of CMOS with FinFET the half adder and full adder the reduction is nearly of 90% and 96 % respectively. The proposed method further improvises about 60% reduction in power for CMOS half adder and about 78% reduction for FinFET. Similarly for full adder its 85% in CMOS and 77% in FinFET. The results of compressor type 1 and compressor type 2 shows the improvement in power reduction by 97% and 98% while using FinFET instead of CMOS. The current analysis is given in the Table 3. for all the components of the proposed design.

TABLE III. POWER ANALYSIS

COMPONENT	AVERAGE POWER in µW		% improvement in Power for proposed Circuits
	CMOS	FinFET	
AND GATE	49.4	1.24	97.49
HALF ADDER	22.9	2.41	89.48
PROPOSED HALF ADDER	9.1	0.528	94.20
FULL ADDER	81.2	2.55	96.86
PROPOSED FULL ADDER	12	0.562	95.32
COMPRESSOR1	49.4	1.24	97.49
COMPRESSOR2	49	1.27	97.41

TABLE IV. CURRENT ANALYSIS

COMPONENT	AVERAGE CURRENT in µA		% improvement in Current for proposed Circuits
	CMOS	FinFET	
AND GATE	26.5	1.24	95.32
HALF ADDER	14.5	1	93.10
PROPOSED HALF ADDER	1.68	0.264	84.29
FULL ADDER	17.7	2.55	85.59
PROPOSED FULL ADDER	4.58	0.298	93.49
COMPRESSOR1	26.5	1.24	95.32
COMPRESSOR2	28.2	1.27	95.50

The energy consumed by different devices is shown in Table 4. The FinFET dominates and outperforms the CMOS in its consumption of energy. The measure of average power consumed is measured for a 4 bit multiplier in 32nm technology. Even though the existing circuits in literature show decreasing average power consumption as the process length is decreased, the proposed FinFET based design consumes least power among the multipliers with more speed. The power consumption is reduced when compared to the existing design. The circuit is further analyzed by executing the circuit using different systolic architecture. Power and energy are observed, performance of CMOS and FinFET based multiplier is shown in the Table 5. The table 5 presents the performance of different multipliers as shown in figure 9, 10, 11 and 12.

CONCLUSION

FinFET based arithmetic circuits for the processing element units with less area and low power is proposed and the results found promising when compared to the existing methods. The proposed arithmetic circuit's half adder, full adder and a multiplier makes the important building blocks of various signal processing algorithms. To reduce the number of operands and partial products a 4-2 compressor based multiplier is proposed in this paper. When comes to complicated interconnects and more components the proposed design reduces the complexity and enhances the way the outputs are projected outside. The embasis on low power is achieved at its maximum level in this work about 96%. The proposed circuits are modelled and simulated using Synopsis HSPICE.

CONFLICT OF INTEREST

The authors declare no conflict of interests.

ACKNOWLEDGEMENT

None

FINANCIAL DISCLOSURE

None

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